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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
QI, ZHI QIANG	

ART UNIT	PAPER NUMBER
2871	

DATE MAILED: 04/22/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/550,282	PARK ET AL.	
	Examiner	Art Unit	
	Mike Qi	2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 March 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-2, 11-16 and 22-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 6,100,954 (Kim et al) in view of US 6,172,728 (Hiraishi) and US 6,061,110 (Hisatake et al).

Claims 1, 15 and 22, Kim discloses (col.1, line 41 – col.5, line 20; Figs.1-6) that a liquid crystal display device comprising:

(concerning claims 1 and 15)

- gate line (15) formed on a transparent substrate (11), the gate line (15) having gate electrodes (13) connected thereto (the gate electrode '13' protruding from the gate line '15'); and a portion protruding from the gate line (15) to serve as a gate electrode (13) of a thin film transistor on a transparent substrate (11);
- source line (25) (data lines) crossing the gate line (15) and formed on the transparent substrate (11);
- gate insulating layer (17) electrically insulating the data line (25) and the gate line (15) (see Fig.6);

- thin film transistor (TFT) formed at an intersection of the gate line (15) and the data line (25), and connected to the gate line (15) and the data line (25);
- a protection film (29) provided by insulating material such as silicon nitride (SiNx) (functions as a passivation layer) formed over the TFT;
- pixel electrode (31) having portions formed on the surface of the protection film (29) (functions as a passivation layer), but not over the TFT;

(concerning claim 22)

- forming a gate line (15) and gate electrode (13) connected thereto on a transparent substrate (11),
- forming gate insulating film (17) over the gate line (15) and the gate electrode (13) (see Figs.6, 2F);
- forming a semiconductor layer (19) over the gate electrode (13);
- forming a date line (25) crossing the gate line (15); and a source electrode (23) connected to the data line (25) and on a first portion (such as left portion) of the semiconductor layer (19), and a drain electrode (27) on second portion (such as right portion) of the semiconductor layer (19);
- forming protection insulating film (29) (functions as a passivation layer) having a contact hole exposing the drain electrode (27) over the transparent substrate (11);

- forming pixel electrode (31) with portions disposed on the protection insulating film (29) (functions as a passivation layer), but not over the TFT, and connected to the drain electrode (27) via the contact hole.

Kim does not expressly discloses that a low reflective layer formed on at least a portion of the gate line or the data line; and no black matrix between the pixel electrode and the upper substrate and above the low reflective layer (no black matrix between the two substrates).

However, Hiraishi discloses (col.6, lines 34-37; Fig.1) that by providing a low-reflective film preferably made of chromium oxide (CrOx) on the gate lines (2) and the source lines (3) (data line), the display quality is enhanced.

Still lacking limitation is such that no black matrix between the two substrates.

However, Hisatake discloses (col.3, lines 46 – 61) that in order to increase the brightness of the reflective liquid crystal display device, no light shielding layer is applied. According to the low reflective layer (such as the material Cr/CrOx having same function as black matrix) formed over the gate line or date line that will suppress the reflectance, such that, inherently, the black matrix is not required so as to increase the display brightness.

Since a low reflective film formed on the gate lines and the data lines would enhance the display quality as Hiraishi taught.

Therefore, it would have been obvious to those skilled in the art at the time the invention was made to form a low reflective layer on at least a portion of the date line or the gate line as claimed in claims 1, 15 and 22 for enhancing the display quality.

Claims 2 and 16, the lacking limitation is such that the low reflective layer formed on gate line.

However, Hiraishi discloses (col.6, lines 34-37; Fig.1) that by providing a low-reflective film preferably made of chromium oxide (CrOx) on the gate lines (2) and the source lines (3) (data line), the display quality is enhanced.

Therefore, it would have been obvious to those skilled in the art at the time the invention was made to form a low reflective layer on at least a portion of the gate line as claimed in claims 2 and 16 for enhancing the display quality.

Claims 11, the lacking limitation is such that the low reflective layer formed on the passivation layer.

However, Hiraishi discloses (col.5, lines 8 –11; col.6, lines 43-44; Fig.2) that an interlayer insulating film (8) (functions as a passivation layer) is formed entirely over the TFT (1), the gate line (2) and the source line (3) (data line), and a pixel electrode (4) is formed on the interlayer insulating film (8) (functions as a passivation layer) and connecting with the drain electrode (14) via contact hole (9a) in the interlayer insulating film (8) (functions as a passivation layer). Hiraishi indicated (col.6, lines 34-37) providing a low-reflective film on the gate lines (2) and the data lines (3), so that the interlayer insulating film (8) (functions as a passivation layer) is also formed over the low-reflective film, and that would enhancing the display quality.

Therefore, it would have been obvious to those skilled in the art at the time the invention was made to use a low reflective layer as claimed in claim 11 for enhancing the display quality.

Claims 12-13, 23-24, the lacking limitation is such that the pixel electrode formed on the data line and the data line.

However, Hiraishi discloses (col.5, lines 56-57; Fig.1) that the pixel electrode (4) is formed over a portion of the data line (3) and over a portion of the gate line (2), and the unnecessary leakage of light to the gap between the pixel electrodes and the gate lines or the date lines is prevented.

Therefore, it would have been obvious to those skilled in the art at the time the invention was made to arrange the pixel electrode over a portion of the gate line or the data line as claimed in claims 12-13, 23-24 for preventing the unnecessary light leakage.

Claims 14 and 25, the lacking limitation is such that the color filter provided on the counter substrate and sealing the two substrates.

However, Hiraishi discloses (col.7, lines 13 – 24) that color film is provided on the counter substrate (20) (color filter substrate) is desired; and a liquid crystal material (30) sealed between the color filter substrate (20) and the transparent substrate (10), such that to display a color image and assembly the liquid crystal display device.

Therefore, it would have been obvious to those skilled in the art at the time the invention was made to use color filter as claimed in claims 14 and 25 for achieving a color image display.

3. Claims 3-4, 6-8, 10, 17-19 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim, Hiraishi and Hisatake as applied to claims 1-2, 11-16 and 22-25

above, and further in view of US 6,503,772 (Ohtsu et al) and US 6,259,200 (Morita et al).

Claims 3-4, 6-8, 10, 17-19 and 21, the lacking limitations is such that TFT electrodes and low reflective layer formed on the electrodes.

However, Hiraishi discloses (col.6, lines 13 – 37; Fig.2) that the thin film transistor (TFT1) includes a gate electrode (12), a source electrode (13) and a drain electrode (14), and a gate electrode (12) protruding from the gate line (2) (see Fig.2, same as the source/drain electrodes, a source electrode (13) protruding from the data line (3)), so that the gate electrode (12) is connected to the gate line (2) and the source electrode is connected to the date line (3). Hiraishi indicates (col.6, lines 34-37; Fig.1) that by providing a low-reflective film preferably made of chromium oxide (CrOx) on the gate lines (2) (the gate electrode is connected to the gate line) and the source lines (3) (data line) (the source electrode is connected to the data line), the display quality is enhanced. Therefore, forming a low reflective layer on the gate electrode and on the source/drain electrodes to enhance the display quality would have been at least an obvious variation.

Furthermore, Ohtsu discloses (col.4, lines 36-42) that by forming the electrode with a low reflectance material, the electrodes and the electrode line can be provided with the same function as the black matrix, so that means forming low reflective layer on the electrodes (gate electrode or source/drain electrode) would improve the contrast as the function of the black matrix.

Furthermore, Morita also discloses the same principle (col.4, lines 51-67) that the top layer of the signal line (such as the material of Al or Ag) will cause its reflectance to be large enough to degrade the quality of image, such that for this reason, a top layer of a material (such as Cr) having a relatively low reflectance is further applied in the Al film to preclude unwanted light reflection, that means would improve the quality of the image display.

Therefore, it would have been obvious to those skilled in the art at the time the invention was made to form a low reflective layer on the gate electrode and on the source/drain electrodes as claimed in claims 3-4, 6-8, 10, 17-19 and 21 for enhancing the display quality.

4. Claims 5, 9 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim, Hiraishi, Hisatake, Ohtsu and Morita as applied to claims 1-4, 6-8, 10-19 and 21-25 above, and further in view of Applicant admitted prior art (AAPA)

Claims 5, 9 and 20, the lacking limitation is such that the low reflective layer has a reflectivity about 3%.

However, AAPA discloses (page 4, lines 2-3 of the specification) that the reflectivity of CrOx is about 3%, and that is the property of a material. Using CrOx as the low-reflective layer, the material CrOx must have such reflectivity, and that would have been at least obvious.

Response to Arguments

5. Applicant's arguments filed on March.15, 2004 have been fully considered but they are not persuasive.

Applicant's **only** arguments are as follows:

1) The references do not teach the pixel electrode does not cover the TFT; and no black matrix between the two substrates as claimed in claims 1, 15 and 22.

Examiner's responses to Applicant's **only** arguments are as follows:

1) The conventional LCD structure such as the references Kim or AAPA (see the Fig.1 of Kim and the Fig.1 of AAPA) teach the pixel electrode does not cover the TFT. The reference Hasatake discloses (col.3, lines 46 – 61) that in order to increase the brightness of the reflective liquid crystal display device, no light shielding layer is applied. According to the low reflective layer (such as the material Cr/CrOx having same function as black matrix) formed over the gate line or date line that will suppress the reflectance, such that, inherently, the black matrix is not required so as to increase the display brightness.

Conclusion

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mike Qi whose telephone number is (571) 272-2299. The examiner can normally be reached on M-T 8:00 am-5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Kim can be reached on (571) 272-2293. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Mike Qi
April 2, 2004

DUNG T. NGUYEN
PRIMARY EXAMINER